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BSCpE 3A

**Synchronous Binary Up Counter**

**VHDL Code:**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity binary\_counter is

Port (rs,clk: in STD\_LOGIC;

q: inout STD\_LOGIC\_VECTOR (3 downto 0));

end binary\_counter;

architecture Behavioral of binary\_counter is

signal div:std\_logic\_vector(22 downto 0);

signal temp:STD\_LOGIC\_VECTOR (3 downto 0);

signal clkd:std\_logic;

begin

process(clk)

begin

if rising\_edge(clk)then

div<= div+1;

end if;

end process;

clkd<=div(22);

process(clkd,rs)

begin

if(rs='1')then temp<=(others=>'0');

elsif(clkd='1' and clkd'event) then

temp<=temp+1;

q<= temp;

end if;

end process;

end Behavioral;